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EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/858,238	CHONG ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 17 OCTOBER 2002.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12,16-24 and 32-45 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 7-12 and 16-18 is/are allowed.

6)☒ Claim(s) 1,2,19,21,22,24,32,34-36,39,40 and 42-45 is/are rejected.

7)☒ Claim(s) 3-6,20,23,33,37,38 and 41 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 15 May 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The present Office Action is responsive to Applicant's amended Response filed October 17, 2002 as Paper No. 3 (Certificate of Mailing date: October 11, 2002). The Examiner acknowledges the amendments to the Specification and Claims 1-3, 5-10, 16, 17, 19-24, 32 and 33, the cancellation of Claims 13-15 and 25-31, and the addition of new Claims 36-45. Accordingly, Claims 1-12, 16-24 and 32-45 remain pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Watanabe et al. (US 4,643,526) Ceresa et al. (US 3,967,162)

Hashimoto (US 6,448,634 B1) Horiuchi et al. (US 6,229,099 B1)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1, 32, 34, 40 and 42-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al.

As to Claim 1, Watanabe et al. discloses, in Fig. 1: an IC 17 having a first dense formation of lands 17a (col.2: 41-45); a substrate 11b comprising: a second dense formation of lands 12c on a surface thereof formed in a geometrical pattern to maximize the density of the second dense formation of lands 12c, while constrained by the size of individual lands 12c and by the width and spacing of substrate traces 13b coupled to the lands 12c; wherein the second dense formation of lands 12c is formed in a pattern comprising a combination of a face center rectangular pattern and a vertical stack pattern: the vertical stack pattern is "face-centered" on substrate 11b; i.e., equidistant from a pair of the sides of substrate 11b (Fig. 1).

As to Claim 32, Watanabe et al. discloses, in Fig. 1: forming lands 12c within a die-bonding area on a surface of substrate 11b in a geometrical pattern to maximize the trace escape density of traces 13b coupled to lands 12c and escaping the die-bonding area on the surface of substrate 11b while constrained by the land size and by the width and spacing of traces 13b, wherein the lands 12c are formed in a vertical stack pattern having at least three or more lands 12c in a vertical stack (i.e., given the land size of lands 12c and the width and spacing of traces 13b, as shown in Fig. 1, the trace escape density of traces 13b from the die-bonding area that corresponds to chip 17 is inherently "maximized" by allowing **all** the traces 13b corresponding to lands 12c--a one-to-one correspondence--to escape from the die-bonding area by including the spaces between

the vertical stacks for routing traces 13b); and coupling lands 17a on an integrated circuit 17 to corresponding lands 12c on the surface of substrate 11b (col.2: 41-44).

As to Claim 34, Watanabe et al. further discloses that IC 17 is an unpackaged die (col.1: 30-32; col.2: 18-20 and 41-44).

As to Claim 40, Watanabe et al. further discloses an IC 17 having first dense formation of lands 17a (col.2: 41-45); a substrate 11b comprising: a second dense formation of lands 12c on a surface thereof, each land having coupled thereto a corresponding substrate trace 13b escaping the die-bonding area (Fig. 1); the second dense formation of lands 12c is formed in a vertical stack pattern having at least one group of three or more lands in a vertical stack (Fig. 1); and wherein substrate traces 13b coupled to corresponding lands 12c in a vertical stack are all located on the same side of the vertical stack (Fig. 1).

As to Claim 42, Watanabe et al. further discloses that the second dense formation of lands 12c comprises a plurality of vertical stacks at the periphery of the surface of substrate 11b (Figs. 1 and 2).

As to Claim 43, Watanabe et al. further discloses that the second dense formation of lands 12c further comprises a face center rectangular pattern: the vertical stack pattern is "face-centered" on substrate 11b; i.e., equidistant from a pair of the sides of substrate 11b (Fig. 1).

As to Claim 44, Watanabe et al. further discloses that the lands 12c are formed as a plurality of vertical stack patterns at the periphery of the surface of substrate 11b (Figs. 1 and 2).

As to Claim 45, Watanabe et al. further discloses that the plurality of vertical stack patterns each comprise at least three lands 12c, and the traces 13b coupled to corresponding lands 12c are all located on the same side of the vertical stack (Fig. 1).

5. Claims 36 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto.

As to Claim 36, Hashimoto discloses: a substrate 1 (Fig. 1) having a die-bonding area (comprising bonding portions 12 and 22 of traces 11 and 21, respectively) on which to mount an IC 40 having a first dense formation of lands 42 (Figs. 3, 4 and 5; col.10: 10-15); the substrate 1 comprising: a second dense formation of lands 15 on a surface thereof, each land 15 having coupled thereto a substrate trace 11 escaping the die-bonding area (Figs. 3 and 4); wherein the second dense formation of lands 15 is formed in an undulating pattern (Figs. 3 and 4).

As to Claim 39, Hashimoto discloses that the second dense formation of lands further comprises a face center rectangular pattern 21 (Figs. 3 and 4).

6. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Horiuchi et al.

Horiuchi et al. discloses : a substrate on which to mount an IC having a first formation of lands (col.2: 22-27; col.7: 9-15); the substrate comprising a second dense formation of lands 10 on a mounting surface thereof formed in a geometrical pattern (plural vertical stack patterns arranged in parallel) to maximize the density of the second dense formation of **lands** 10 (the arrangement of the plurality of vertical stack patterns evidently "maximizes" the **land density** of the second dense formation of lands 10 on the first surface shown in Fig. 2, as compared to the lesser **land densities** on the inner layers shown in Figs. 3-6 wherein intermediate lands 10 have been selectively removed in order to increase the trace escape density on the inner layers) while constrained by the size of individual lands 10 and by the width and spacing of substrate traces 7 coupled to the lands 10 (col.6: 42-col.7: 6); wherein the second dense formation of lands 10 is formed in a pattern comprising a combination of a face center rectangular pattern (pads 10a are symmetrically centered on the substrate) and the vertical stack pattern (see Fig. 2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 19, 21, 22, 24 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al.

As to Claim 19:

I. Watanabe et al. discloses, in Fig. 1: forming on a surface of substrate 11b a plurality of traces 13b, the traces 13b having at least a width and a spacing from one another; forming within a die-bonding area on the surface of substrate 11b a plurality of lands 12c, each land 12c coupled to a corresponding one of the plurality of traces 13b, and each having at least a size, the plurality of traces 13b escaping the die-bonding area, the plurality of lands 12c being formed in at least one geometrical pattern (i.e., a vertical stack pattern having at least three or more lands in a vertical stack) that maximizes the trace escape density while constrained by the land size and by the width and spacing of the traces: i.e., given the land size of lands 12c and the width and spacing of traces 13b, as shown in Fig. 1, the trace escape density of traces 13b from the die-bonding area that corresponds to chip 17 is inherently "maximized" by allowing **all** the traces 13b corresponding to lands 12c (a one-to-one correspondence) to escape from the die-bonding area by including the spaces between the vertical stacks for routing traces 13b.

II. Watanabe et al. does not specify a "predetermined" width and spacing of traces 13b and does not specify a "predetermined" size of lands 12c.

III. However, given the chip electrode density of LSI chip 17 and the layout positioning and geometry of the LCD panel electrodes, to which the substrate 11b is connected (Fig. 1; col.1: 6-9), it would have been obvious to one of ordinary skill in the art at the time the invention was made to predetermine said width, spacing and size dimensions as part of the fabrication process of substrate 11b in Watanabe et al. in

order to effectively perform the disclosed plating, or thick/thin film processing of the circuitry (col.2: 31-37) so that the layout of traces 13b and lands 12c meet the circuit layout specifications--e.g., connection to LCD panel electrodes, usage of given board real estate, desired trace resistivity, given chip electrode density, etc.--required by the application.

As to Claim 21, Watanabe et al. further discloses that the lands 12c are formed as a plurality of vertical stack patterns at the periphery of the surface of substrate 11b (Figs. 1 and 2).

As to Claim 22, Watanabe et al. further discloses that the plurality of vertical stack patterns each comprise at least three lands 12c, and substrate traces 13b coupled to corresponding lands 12c in each vertical stack are all located on the same side of the vertical stack (Fig. 1).

As to Claim 24, Watanabe et al. further discloses that the at least one geometrical pattern further comprises a "face center rectangular pattern:" that is, the vertical stack pattern is "face-centered" on substrate 11b; i.e., equidistant from a pair of the sides of substrate 11b (Fig. 1).

As to Claim 35:

I. Watanabe et al. prefers the use of an unpackaged IC die for direct mounting onto the substrate in order to enable a compact assembly but also discloses that packaged IC die are conventional in the pertinent art of Watanabe et al., said packaged IC die having the disadvantage of not permitting the package to be as compact as possible (col.1: 20-23 and 30-32).

II. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a packaged IC for applications in the pertinent art of Watanabe et al. wherein the packaging (i.e., a chip carrier) may provide, as is well-known in the art the following advantages in certain applications where compact assembly is not absolutely critical: 1) greater circuit density and functionality; and/or 2) a less dense I/O package (i.e., carrier) footprint than the more dense I/O bump contact array of the unpackaged die mounted thereon (the package functioning as an adapter board), thus enabling the electrical connection of the high density IC die to a substrate with contact pads having a less dense footprint of contacts matching that of the chip carrier package, said less dense footprint of contacts having a larger contact pad pitch which facilitates and ensures a more reliable solder bonding of the packaged IC die to the substrate.

9. Claims 1, 19, 21, 22, 24, 32, 34, 35, 40 and 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ceresa et al.

As to Claim 1:

I. Ceresa et al. discloses, in Figs. 1-3: a substrate 20 on which to mount a device 12 having a first dense formation of lands 16: the substrate comprising: a second dense formation of lands 26a on a surface thereof formed in a geometrical pattern (i.e., a vertical stack pattern having at least three or more lands 26a in a vertical stack; Fig. 2) to maximize the trace escape density of traces 24 coupled to lands 26a and escaping the device-bonding area on the surface of substrate 20 (Figs. 1 and 2; col.3: 42-48 and 61-63) while constrained by the size of the individual lands 26a and by the width and

spacing of traces 24 (Fig. 1; col.3: 55-63) coupled to lands 26a; the second dense formation of lands 26a is formed in a pattern comprising a combination of a face center rectangular pattern and a vertical stack pattern ("face-centered" with respect to the sides of substrate 20 perpendicular to the vertical stacks of lands 26a; Figs. 1 and 2).

II. Ceresa et al. does not identify the bonding area on substrate 20 as a die-bonding area or device 12 as an IC die; rather, Ceresa et al. discloses that element 12 is a circuit board (like element 14; col.2: 60-66). However, Ceresa et al. also discloses that elements 12 and/or 14 may also be micro-electronic (i.e., IC) devices (col.1: 7-16; col.2: 64) instead of circuit boards.

III. Since Ceresa et al. teaches the assembly of circuit substrates in general (boards or devices), it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device-bonding area on the surface of substrate 20 so that it is, in particular, a die-bonding area for receiving a micro-electronic (IC) device die with lands 16 (Figs. 1 and 3) for mechanical (bonding) and electrical connection to lands 26a of substrate 20 in order to complete the assembly of a micro-electronic device (Fig. 3), as taught by Ceresa et al.

As to Claim 19:

I. Ceresa et al. discloses, in Figs. 1-3: forming on a surface of a substrate 20 a plurality of traces 24, the traces 24 having at least a predetermined width and a predetermined spacing from one other (col.3: 18-25, 33-38 and 57-61); and forming within a device-bonding area on the surface of substrate 20 a plurality lands 26a, each coupled to a corresponding one of the plurality of traces 24 (see the **top half portion** of

sheet 22 above the dotted fold-line in Fig. 2; it is this **top half portion** of sheet 22, with its lands 26a and corresponding traces 24, that is placed on the device-bonding surface area of substrate 20 that carries device 14; see Figs. 2 and 3, and col.3: 42-54), and each land 26a having at least a predetermined size (col.4: 12-17); the plurality of traces 24 escaping the device-bonding area (Figs. 1 and 2; col.3: 42-48 and 61-63); the plurality of lands 26a formed in at least one geometrical pattern (i.e., a vertical stack pattern having at least three or more lands 26a in a vertical stack; Fig. 2) that maximizes the trace escape density while constrained by the size of lands 26a and by the width and spacing of traces 24 (Fig. 1; col.3: 55-63).

II. Ceresa et al. does not identify the bonding area on substrate 20 as a die-bonding area; rather, Ceresa et al. discloses that element 12 is a circuit board (like element 14; col.2: 60-66). However, Ceresa et al. also discloses that elements 12 and/or 14 may also be micro-electronic devices (col.1: 7-16; col.2: 64) instead of circuit boards.

III. Since Ceresa et al. teaches the assembly of circuit substrates in general (boards or devices), it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device-bonding area on the surface of substrate 20 so that it is, in particular, a die-bonding area for receiving a micro-electronic device die with lands 16, such as those in circuit substrate 12 (Figs. 1 and 3) for mechanical (bonding) and electrical connection to lands 26a of substrate 20 in order to complete the assembly of a micro-electronic device, as taught by Ceresa et al.

As to Claim 21, Ceresa et al. further discloses that lands 26a are formed as a plurality of vertical stack patterns at the periphery of the surface of substrate 20 (Fig. 1).

As to Claim 22, Ceresa et al. further discloses that the plurality of vertical stack patterns each comprise at least three lands (i.e., the lands 26a on the top half portion of sheet 22 in Fig. 2, said vertical stacks of lands 26a being positioned on the surface of substrate 20, as shown in Fig. 1), and wherein the substrate traces 24 coupled to corresponding lands 26a in each vertical stack are all located on the same side of the vertical stack (Fig. 2).

As to Claim 24, Ceresa et al. further discloses, in Fig. 1, that the at least one geometrical pattern (i.e., the at least one vertical stack pattern) comprises a face center rectangular pattern (i.e., "face-centered" with respect to the sides of substrate 20 perpendicular to the vertical stacks of lands 26a).

As to Claim 32:

I. Ceresa et al. discloses, in Figs. 1-3: forming within a device-bonding area on the surface of substrate 20 in a geometrical pattern (i.e., a vertical stack pattern having at least three or more lands 26a in a vertical stack) to maximize the trace escape density of traces 24 coupled to lands 26a and escaping the device-bonding area on the surface of substrate 20 (Figs. 1 and 2; col.3: 42-48 and 61-63) while constrained by the size of lands 26a and by the width and spacing of traces 24 (Fig. 1; col.3: 55-63); coupling lands 16 on device or circuit board 12 to corresponding lands 26a on substrate surface 20.

II. Ceresa et al. does not identify the bonding area on substrate 20 as a die-bonding area or device 12 as an IC die; rather, Ceresa et al. discloses that element 12 is a circuit board (like element 14; col.2: 60-66). However, Ceresa et al. also discloses that elements 12 and/or 14 may also be micro-electronic (i.e., IC) devices (col.1: 7-16; col.2: 64) instead of circuit boards.

III. Since Ceresa et al. teaches the assembly of circuit substrates in general (boards or devices), it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device-bonding area on the surface of substrate 20 so that it is, in particular, a die-bonding area for receiving a micro-electronic (IC) device die with lands 16 (Figs. 1 and 3) for mechanical (bonding) and electrical connection to lands 26a of substrate 20 in order to complete the assembly of a micro-electronic device (Fig. 3), as taught by Ceresa et al.

As to Claims 34 and 35:

I. Ceresa et al., as modified to include a die-bonding area for receiving a micro-electronic device die, is silent as to a micro-electronic device die that is packaged or unpackaged.

II. However, since die bonding techniques like chip-on-board or flip-chip (as taught in Fig. 3 of Ceresa et al.) are known in the art as techniques for directly mounting the electrodes of an unpackaged die on a circuit board substrate, and since flip-chip bonding is also used for mounting the carrier electrodes of a packaged die (i.e., a die mounted on a carrier substrate) to a circuit board substrate, it would have been obvious

to one of ordinary skill in the art to modify the substrate element 12 to be an unpackaged or packaged die in accordance with the requirements of the application.

As to Claim 40:

Ceresa et al. discloses, in Figs. 1-3: a substrate 20 having a device-bonding area on which to mount a device or circuit board 12 having a first dense formation of lands 16; substrate 20 comprising: a second dense formation of lands 26a on a surface thereof, each land 26a having coupled thereto a corresponding substrate trace 24 escaping the device-bonding area (Figs. 1 and 2; col.3: 42-48 and 61-63); wherein the second dense formation of lands 26a is formed in a vertical stack pattern having at least on group of three or more lands in a vertical stack (Fig. 2); wherein the substrate traces 24 coupled to corresponding lands 26a in a vertical stack are all located on the same side of the vertical stack (Figs. 2 and 3).

II. Ceresa et al. does not identify the bonding area on substrate 20 as a die-bonding area or device 12 as an IC die; rather, Ceresa et al. discloses that element 12 is a circuit board (like element 14; col.2: 60-66). However, Ceresa et al. also discloses that elements 12 and/or 14 may also be micro-electronic (i.e., IC) devices (col.1: 7-16; col.2: 64) instead of circuit boards.

III. Since Ceresa et al. teaches the assembly of circuit substrates in general (boards or devices), it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device-bonding area on the surface of substrate 20 so that it is, in particular, a die-bonding area for receiving a micro-electronic (IC) device die 12 with lands 16 (Figs. 1 and 3) for mechanical (bonding) and

electrical connection to lands 26a of substrate 20 in order to complete the assembly of a micro-electronic device (Fig. 3), as taught by Ceresa et al.

As to Claim 42, Ceresa et al. further discloses that the second dense formation of lands 26a comprises a plurality of vertical stacks at the periphery of the surface of substrate 20 (Fig. 1).

As to Claim 43, Ceresa et al. further discloses, in Fig. 1, that the second dense formation of lands 26a comprises a face center rectangular pattern (i.e., "face-centered" with respect to the sides of substrate 20 perpendicular to the vertical stacks of lands 26a).

As to Claim 44, Ceresa et al. further discloses that lands 26a are formed as a plurality of vertical stack patterns at the periphery of the surface of substrate 20 (Fig. 1).

As to Claim 45, Ceresa et al. further discloses that the plurality of vertical stack patterns each comprise at least three lands 26a, and wherein the traces 24 coupled to corresponding lands 26a in each vertical stack are all located on the same side of the vertical stack (Figs. 1 and 2).

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al.

I. Horiuchi et al. discloses an equation that models an efficient arrangement of pads and traces that optimize the routing (escape density) of traces 7 from the vertically stacked land patterns in the mounting layer (Fig. 2) and the inner layers (Figs. 3-6) of the multilayer board (col.6: 66-67). *IMPORTANT NOTE*: The equation in col.6: 66-67 should read as *m={(land pitch)x(n-1)-(land diameter)-(Ts)}/(Tw+Ts);*

where *m* is the number of traces that can be passed between the lands at the ends of an arrangement of *n* lands (col.3: 1-16), *n* is the number of lands in an arrangement of lands, *Tw* is trace width and *Ts* is the space between traces. The "+" sign wrongly placed before the final parenthetical sum (see col.6, line 67) should be a division sign "/", as evidenced by the computation in col.7, line 1.

II. Horiuchi et al. does not teach a **maximum** trace escape density formula in particular but nevertheless allows for the case wherein the value of the numerator in the above-mentioned circuit arrangement equation may be unity; i.e., *{(land pitch)x(n-1)-(land diameter)-(Ts)} = 1.*

III. Since Horiuchi et al. neither limits the numerator to any particular optimal subset of positive integer values nor absolutely precludes certain other positive integer values, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set the pitch, diameter and spacing values such that *{(land pitch)x(n-1)-(land diameter)-(Ts)} = 1* for circuit board applications wherein the number *m* of traces (i.e., "circuit patterns") that can be passed through the space between the lands at both ends of an arrangement of plural vertical stacks (col.6: 47-48) must be the quantity 1/(Tw + Ts) according to the above-mentioned circuit arrangement equation, which would inherently be the maximum trace escape density of traces 7.

Response to Arguments

11. Applicant's arguments with respect to Claims 1-5, 7-15, 19-23, and 25-35 have been considered but are moot in view of the new ground(s) of rejection. The new

grounds of rejection include withdrawing the previously indicated allowable subject matter (see Office Action of July 18, 2002, Paper No. 2, p.13, section 11) due to prior art newly discovered by the Examiner. Accordingly, the present Office Action has been made NON-FINAL.

12. Regarding the Applicant's remark concerning their Specification's support for increasing or maximizing the land density, on p.15 (the final full paragraph) of the above-cited instant amended Response (Paper No. 3), the Examiner notes that Claim 1 recites "a geometrical pattern to maximize the density of the second dense formation of lands." The Horiuchi et al. reference relied upon for the rejection of Claim 1, above, clearly reads on the maximization of the Applicant's claimed **land density** on the surface layer of the substrate since the surface layer arrangement of parallel vertical stacks maximizes the number of lands on the surface layer as compared to the inner layers of the multilayer board wherein some lands are removed from the vertical stacks arrangement. Accordingly, the **land densities** of the inner layers are necessarily less than the **land density** of the surface layer of the multilayer board patterned with the parallel vertical stacks. The pattern of parallel vertical stacks evidently maximizes the **land density** of the circuit arrangement on the surface of the multilayer board.

Allowable Subject Matter

13. Claims 7-12 and 16-18 have been allowed.

14. Claims 3-6, 20, 23, 33, 37, 38 and 41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 20, 33, 37 and 41 patentability resides in the limitation wherein *the maximum trace escape density equals the reciprocal of (Tw + Ts), wherein Tw equals the width of the substrate traces and Ts equals the spacing between the substrate traces*, in combination with the other limitations of Claims 2, 20, 33, 37 and 41, respectively.

As to Claims 3-4, patentability resides in the limitation wherein *the second dense formation of lands is formed in a pattern comprising a combination of a face center rectangular pattern and a zigzag pattern having a plurality of zigzag rows*, in combination with the other limitations of the broadest claim, Claim 3.

As to Claim 5, patentability resides in the limitation wherein *the second dense formation of lands is formed in a pattern comprising a combination of a face center rectangular pattern and an undulating pattern*, in combination with the other limitations of the claim.

As to Claim 6, patentability resides in the limitation wherein *the second dense formation of lands is formed in a pattern comprising a combination of a face center rectangular pattern and a wave pattern*, in combination with the other limitations of the claim.

As to Claims 7-12, patentability resides in *a second dense formation of lands formed in an undulating pattern*, in combination with the other limitations of base Claim 7.

As to Claims 16-18, patentability resides in *a second dense formation of lands formed in an undulating pattern*, in combination with the other limitations of base Claim 16.

As to Claim 23, patentability resides in the limitation wherein *the at least one geometrical pattern further comprises an undulating pattern*, in combination with the other limitations of the claim.

As to Claim 38, patentability resides in the limitation wherein *the second dense formation of lands comprises a* ***plurality*** *of undulating rows at the periphery of the surface of the substrate*, in combination with the other limitations of the claim.

16. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arima et al. (US 6,479,758 B1) discloses a wiring board with lands, power supply traces and signal traces optimally arranged such that crosstalk is prevented and wiring board size is not necessarily increased (col.1; 66-col.2; 4). The equation that models

this optimal wiring relationship is $k \leq 1+(P-A-S)/(S+W)$, where k is the number of signal lands that are arranged in columns, P is the pitch between signal lands, W is the width of the traces connected to the lands and S is the minimum dimension of a space between two adjacent traces (Fig. 3; col.2: 26-42; col.6: 26-67).

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
January 22, 2003